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PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
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**APPLICANTS: Shimizu Masahiro; Tanaka Yoshinori; Arima Hideaki;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A DIV OF 09/452,099 12/02/1999
WHICH IS A DIV OF 09/119,053 07/20/1998 PAT 6,066,881

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 10-017232(P) 01/29/1998

PG-PUB | DO NOT PUBLISH ☐ | RESCIND ☐

Foreign priority claimed ☐ yes ☐ no
35 USC 119 conditions met ☐ yes ☐ no
Verified and Acknowledged Examiners's intials

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TITLE : Integrated circuit having a memory cell transistor with a gate oxide layer which is thicker than the gate oxide layer of a peripheral circuit transistor

U.S DEPT OF COMM./PAT & TM-PTO-436L/Rev 12-94

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid			DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER		Primary Examiner / PREPARED FOR ISSUE	Application Examiner

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